CLAIMS

What is claimed is:

1. A method comprising:

periodically stalling issuance of input/output (I/O) device accesses by a program in a multiple-processor computer system; and during the stalling step

completing pending I/O device reads.

2. The method as defined in claim 1 wherein periodically stalling further comprises entering an interrupt mode by each processor in the multiple-processor system.

3. The method as defined in claim 2 wherein entering an interrupt mode further comprises entering the interrupt mode by each of the processors substantially simultaneously.

4. The method as defined in claim 1 wherein after completing pending I/O device reads, the method further comprises allowing each processor in the multiple-processor to resume issuing I/O device accesses.

5. The method as defined in claim 4 wherein allowing each processor to resume issuing I/O device accesses further comprises asserting a resume flag associated within each processor by a processor designated as primary.

6. The method as defined in claim 5 wherein asserting a resume flag further comprises asserting a resume flag in a port logic of each of the processors.

7. The method as defined in claim 5 wherein asserting a resume flag further comprises asserting a resume flag in a read/write portion of a memory coupled to each of the processors.

8. A computer system comprising:

a plurality of processors coupled to each other;

at least one of the plurality of processors coupled to an input/output (I/O) device by way of a bridge logic device; and

wherein each of the plurality of processors periodically executes a program that operates to cease issuance of I/O device writes until pending I/O device reads complete.

9. The computer system as defined in claim 8 further comprising:

a plurality of flag registers associated one each with the plurality of processors; and

wherein at least some of the plurality of processors resume issuance of I/O device writes upon assertion of their associated flag registers.

10. The computer system as defined in claim 9 wherein each flag register is external to each processor.

11. The computer system as defined in claim 10 further comprising:

a plurality of memory devices coupled one each to at least some of the plurality of processors;

wherein each flag register is in a local memory of each processor.

12. The computer system as defined in claim 9 wherein each flag register is internal to each processor.

13. The computer system as defined in claim 12 wherein each processor further comprises a port logic, and wherein the flag register is located within the port logic.

14. The computer system as defined in claim 8 further comprising:

one of the plurality of processors designated a primary processor; and

wherein the primary processor is programmed to issue a read to the bridge logic device after cessation of I/O device writes, and wherein when the read to the bridge device completes the primary processor is further programmed to allow the computer system to resume issuance of I/O device writes.

15. A processor comprising:

a core region;

a memory controller; and

a port logic coupled to the core region and the memory controller;

wherein the processor periodically enters an interrupt mode, and during the interrupt mode the processor executes firmware that operates to stop production of input/output (I/O) device write requests.

16. The processor as defined in claim 15 wherein the port logic further comprises a register, and wherein the processor exits the interrupt mode and resumes production of I/O device writes when the register is asserted.

17. The processor as defined in claim 15 wherein during the interrupt mode the processor issues read commands to each bus bridge to which the processor is coupled if the processor has a primary designation.

18. The processor as defined in claim 17 wherein during the interrupt mode the processor commands other processors to resume production of I/O device write requests if the processor has a primary designation.

19. A computer system comprising:

a plurality of means for executing programs and instructions coupled to each other, each processor coupled to a means for storing data and instructions local each of the plurality of means for executing;

at least one of the plurality of means for executing coupled to a means for receiving data from devices external to the computer system and for

sending data to device external to the computer system, the means for receiving coupled to the at least one plurality of means for executing by way of a means for bridging a first and second communication bus; and

wherein each of the plurality of means for executing periodically executes programs that operate to cease issuance of writes to the means for receiving until pending writes to the means for receiving complete.

20. The computer system as defined in claim 19 further comprising:

a plurality of means for triggering associated one each with the plurality of means for executing; and

wherein at least some of the plurality of means for executing resume issuance of writes to the means for receiving upon assertion of their associated means for triggering.

21. The computer system as defined in claim 20 wherein each means for triggering is in the means for storing coupled to each means for executing.

22. The computer system as defined in claim 20 wherein each means for triggering is in its associated means for executing.